ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit comprises a plurality of combinational logic components, a memory and a testing arrangement for configuring the memory prior to testing the combinational logic components using one or more scan chains. The arrangement comprises a bit pattern generator for generating a predetermined bit pattern for writing to the memory, a switching arrangement for selectively switching the memory input to receive data from the combinational logic components or from the data generator. The switching arrangement and data generator are arranged to input the predetermined bit pattern to the memory prior to testing the integrated circuit.